C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC40160BP, TC40161BP, TC40162BP, TC40163BP

SYNCHRONOUS PROGRAMMABLE 4-BIT COUNTER

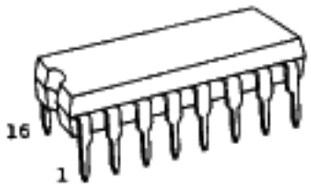
TC40160BP DECADE WITH ASYNCHRONOUS CLEAR

TC40161BP BINARY WITH ASYNCHRONOUS CLEAR

TC40162BP DECADE WITH SYNCHRONOUS CLEAR

TC40163BP BINARY WITH SYNCHRONOUS CLEAR

The TC40160BP, TC40161BP, TC40162BP, and TC40163BP are synchronously programmable 4-bit counters. The TC40160BP and TC40161BP are decimal counter and 4-bit binary counter respectively having asynchronous clear function which directly clears all the flip-flop outputs. The TC40162BP and TC40163BP are decimal counter and 4-bit binary counter respectively which are synchronous at the rising edges of clocks. CLEAR and LOAD of these counters are active at the "L" level. Further, these counters are functionally compatible with the 74160, 74161, 74162, and 74163 of TTL.

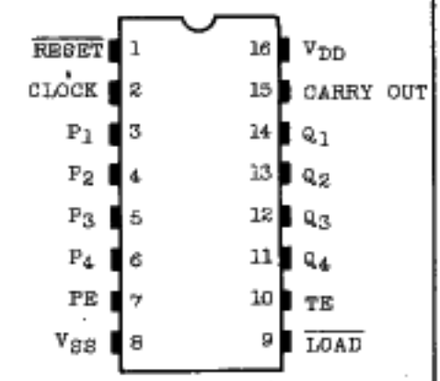


DIP 16(3D16A-P)

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



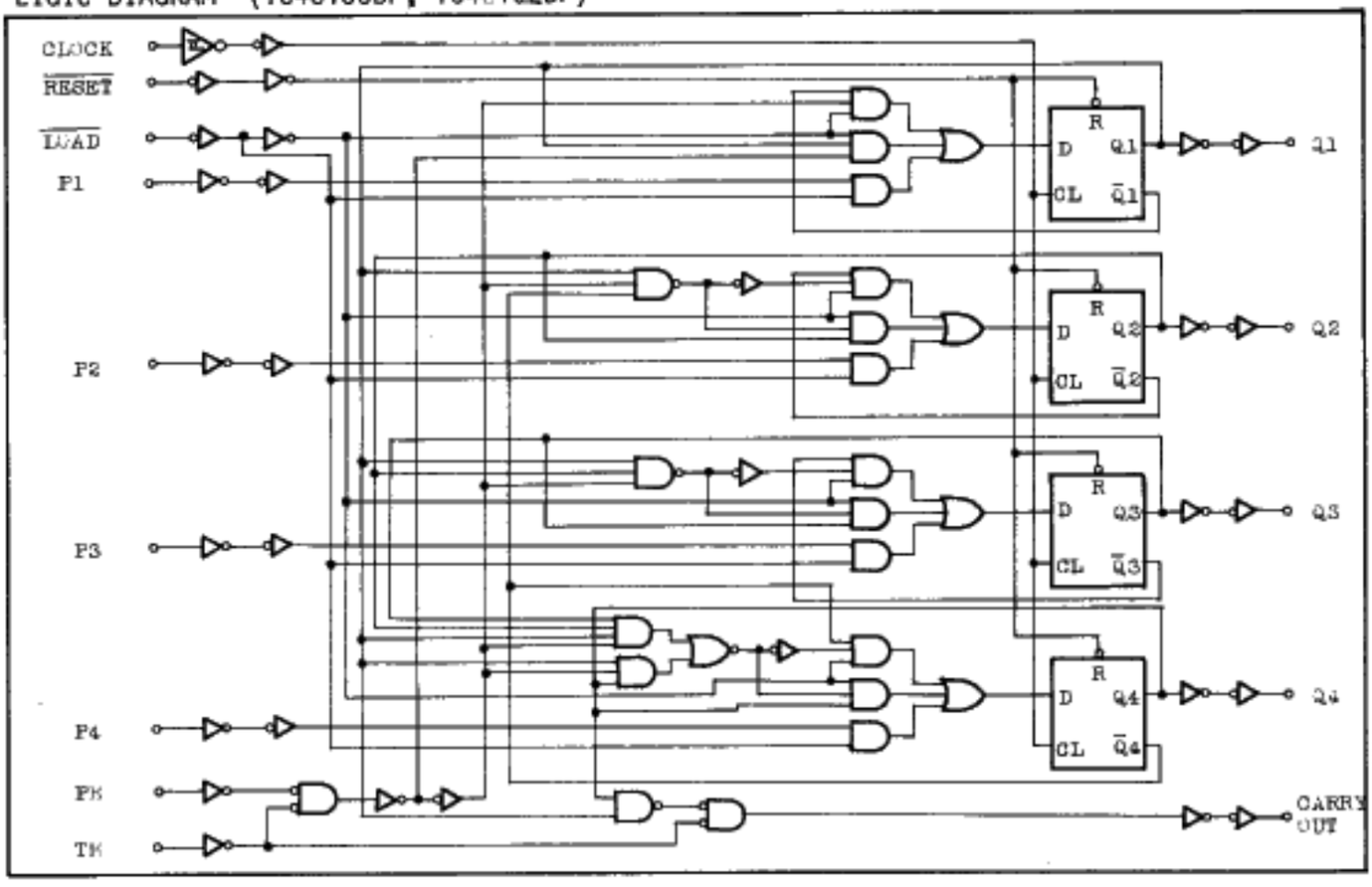
(TOP VIEW)

TRUTH TABLE

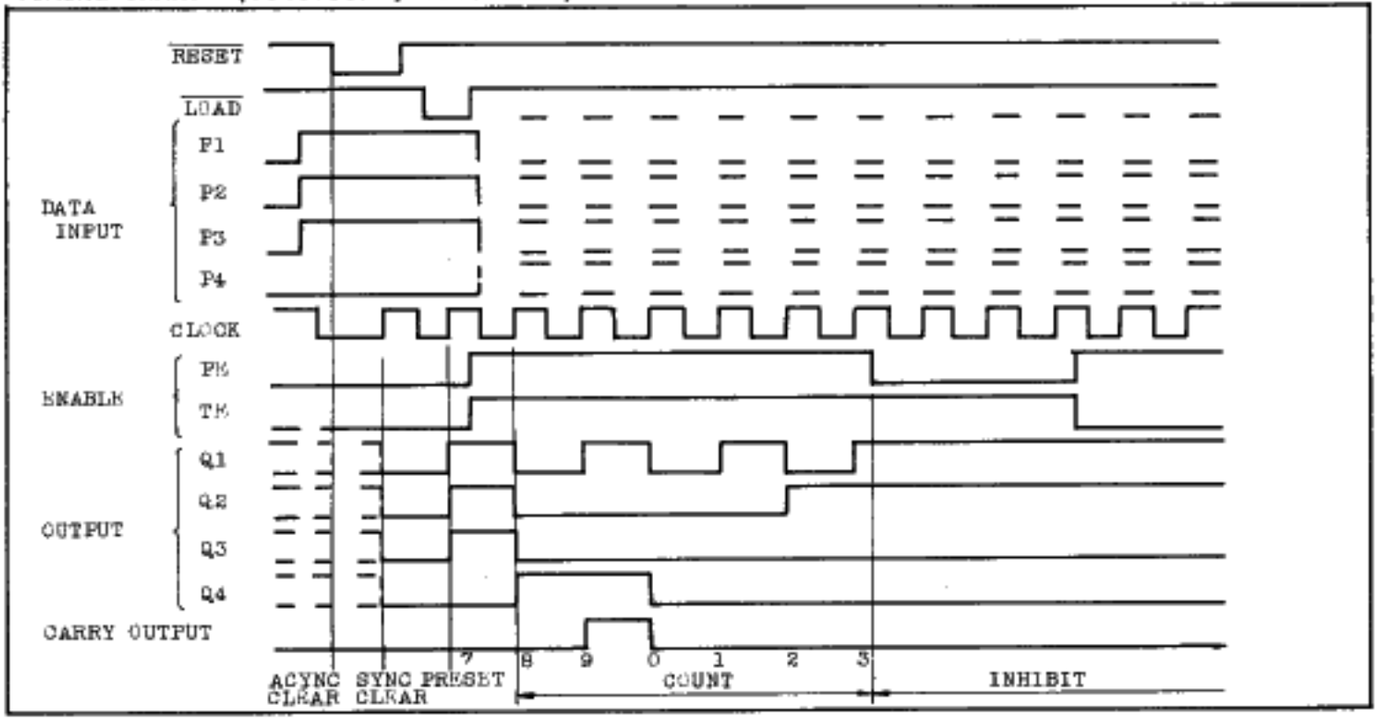
INPUT									OUTPUT			
CLOCK	RESET	LOAD	PE	TE	P_1	P_2	P_3	P_4	Q_1	Q_2	Q_3	Q_4
☆	L	*	*	*	*	*	*	*	L	L	L	L
△ ∫	H	L	*	*	D_1	D_2	D_3	D_4	D_1	D_2	D_3	D_4
△ ∫	H	H	L	L	*	*	*	*	·	·	·	·
△ ∫	H	H	L	H	*	*	*	*	·	·	·	·
△ ∫	H	H	H	L	*	*	*	*	·	·	·	·
△ ∫	H	H	H	H	*	*	*	*	COUNT			
△ ⌊	H	*	*	*	*	*	*	*	·	·	·	·

* : Don't care
△ : Level change
· : No change
D : Data "H" or "L"
☆ : Don't care (TC40160, TC40161); Rise edge (TC40162, TC40163)

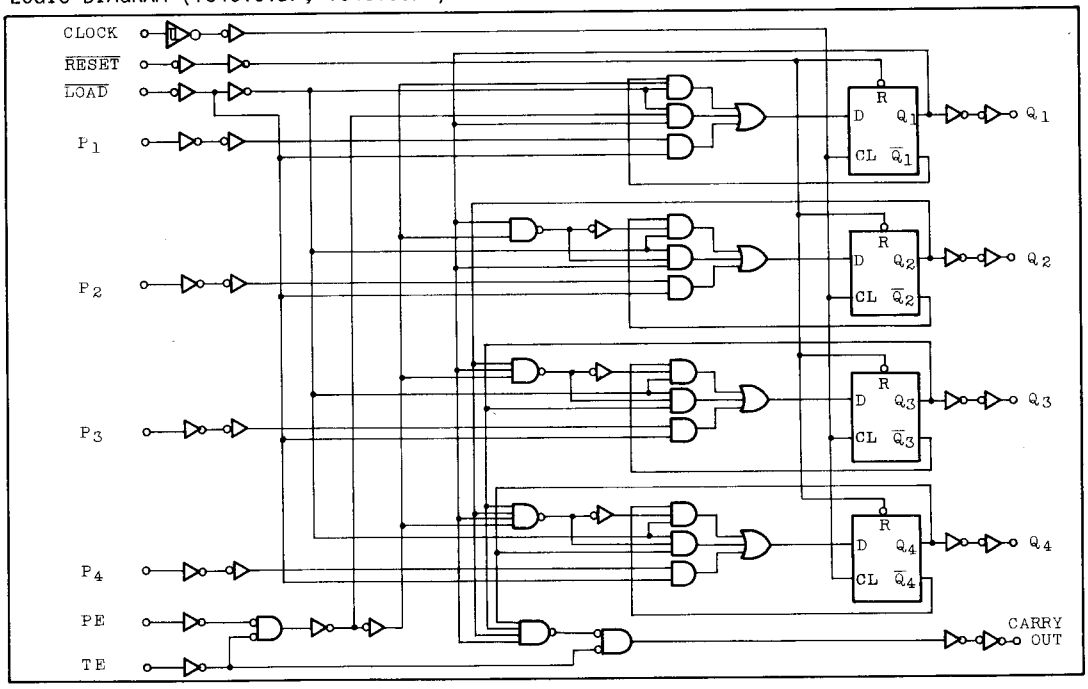
LIGIC DIAGRAM (TC40160BP, TC40162BP)



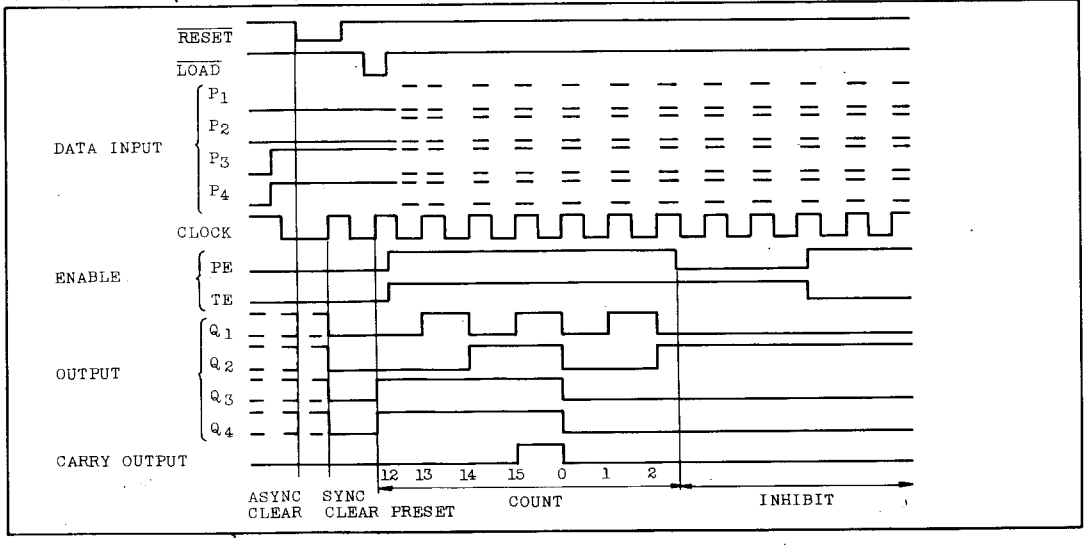
TIMING CHART (TC40160BP, TC40162BP)



LOGIC DIAGRAM (TC40161BP, TC40163BP)



TIMING CHART (TC40161BP, TC40163BP)



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage		V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
			$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
			$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Output Low Current		I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
			V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
			V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
			$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage		V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	→	3.5	-	V
			V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			$\|I_{OUT}\|<1\mu A$									
Input Low Voltage		V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
			V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			$\|I_{OUT}\|<1\mu A$									
Input Current	"H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
	"L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
				MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Quiescent Device Current	I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	5	-	0.005	5	-	150	μA
			10	-	10	-	0.010	10	-	300	
			15	-	20	-	0.015	20	-	600	

* All Valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

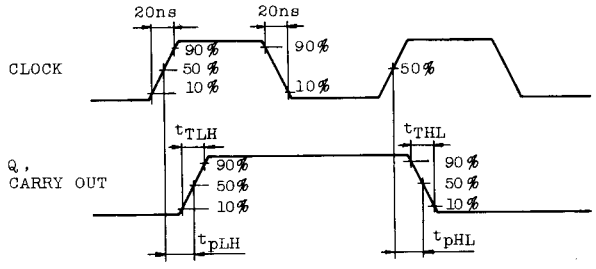
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	250	500	ns
			10	-	100	200	
			15	-	70	140	
Propagation Delay Time (CLOCK-CARRY OUT)	t_{pLH} t_{pHL}		5	-	300	600	
			10	-	120	240	
			15	-	80	160	
Propagation Delay Time (TE-CARRY OUT)	t_{pLH} t_{pHL}		5	-	170	340	
			10	-	65	130	
			15	-	45	90	
Propagation Delay Time ($\overline{RESET}$ - Q) 40160, 40161 Only	t_{pHL}		5	-	180	500	
			10	-	75	220	
			15	-	55	160	
Min. Clock Pulse Width	t_w		5	-	130	250	ns
			10	-	45	90	
			15	-	30	60	
Min. Pulse Width ($\overline{RESET}$) 40160, 40161 Only	t_{WL}		5	-	140	280	
			10	-	55	110	
			15	-	35	70	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

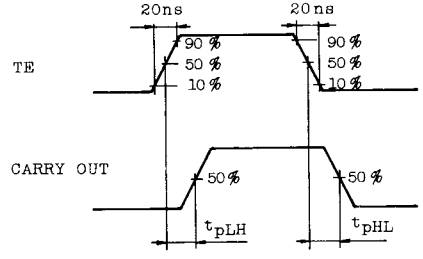
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Max. Clock Frequency	f_{CL}		5	2	4	-	MHz
			10	5.5	11	-	
			15	8	16	-	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	No Limit			μs
			10				
			15				
Min. Set-up Time (P_n - CLOCK)	t_{SU}		5	-	55	240	ns
			10	-	20	90	
			15	-	15	60	
Min. Set-up Time ($\overline{LOAD}$ - CLOCK)	t_{SU}		5	-	75	240	
			10	-	30	90	
			15	-	20	60	
Min. Set-up Time (PE, TE - CLOCK)	t_{SU}		5	-	190	380	
			10	-	70	140	
			15	-	50	100	
Min. Set-up Time ($\overline{RESET}$ - CLOCK) 40162, 40163 Only	t_{SU}		5	-	50	310	
			10	-	20	110	
			15	-	15	70	
Min. Hold Time (P_n, $\overline{LOAD}$, PE, TE-CLOCK)	t_H		5	-	-	0	ns
			10	-	-	0	
			15	-	-	5	
Min. Hold Time ($\overline{RESET}$ - CLOCK) 40162, 40163 Only	t_H		5	-	-30	0	
			10	-	-10	0	
			15	-	-5	0	
Min. Removal Time ($\overline{RESET}$ - COLCK) 40160, 40161 Only	t_{rem}		5	-	80	200	ns
			10	-	25	100	
			15	-	15	70	
Input Capacitance	C_{IN}			-	5	7.5	pF

WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

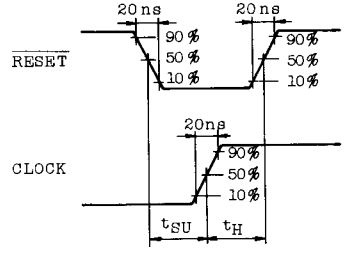
WAVEFORM 1



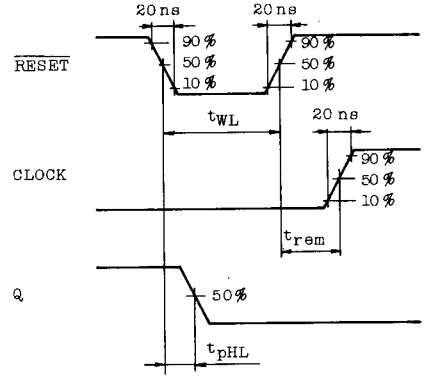
WAVEFORM 2



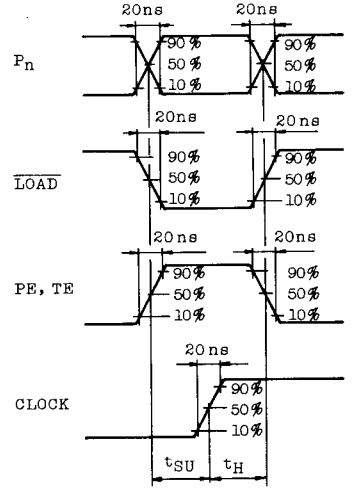
WAVEFORM 3 (40162, 40163)



WAVEFORM 4 (40160, 40161)



WAVEFORM 5



APPLICATION CIRCUIT

1. Cascaded counter packages in the parallel-clocked mode.